Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **IN/OUT A**
2. **OUT/IN A**
3. **OUT/IN B**
4. **IN/OUT B**
5. **CONTROL B**
6. **CONTROL C**
7. **VSS**
8. **IN/OUT C**
9. **OUT/IN C**
10. **OUT/IN D**
11. **IN/OUT D**
12. **CONTROL D**
13. **CONTROL A**
14. **VDD**

**.047”**

**.042”**

**3 2 1 14 13**

**12**

**11**

**4**

**5**

**6 7 8 9 10**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0035” X .0035”**

**Backside Potential: VDD or FLOATING**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .042” X .047” DATE: 8/25/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .015” P/N: CD4016B**

**DG 10.1.2**

#### Rev B, 7/1